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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HUANG, WEN WU	
ART UNIT	PAPER NUMBER
2618	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/772,644	DEMIR ET AL.	
	Examiner	Art Unit	
	WEN W. HUANG	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-7 and 16 are pending.

Claims 8-15 are cancelled.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 4, 5, 7 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nassiri-Toussi et al. (US. 7,194.011 B1; hereinafter "Nassiri") in view of Frigon (US. 7,173,992 B2) and Yamaguchi (US Pub No. 2003/0119444 A1).

Regarding **claim 1**, Nassiri teaches a method for wireless communication initiation for a wireless transmit/receive unit (WTRU) configured to communicate with base stations of a wireless system the WTRU receives an identifying synchronization channel (SCH) signal from at least one base station at a predetermined chip rate in a selected portion of a system time frame (see Nassiri, abstract; col. 6, lines 50-55), the method comprising the steps of:

receiving a wireless signal including at least one SCH signal (see Nassiri, col. 6, lines 1-5);

identifying received SCH signals using a power threshold (see Nassiri, fig. 3, primary search stage 222, col. 8, lines 4-15, peak detector 350) based on a plurality of chip samples sampled at twice the chip rate (see Nassiri, col. 6, lines 53-54);

selecting an identified SCH signal for decoding (see Nassiri, col. 8, lines 16-25, highest peak); and

decoding the selected SCH signal to determine system time frame timing and base station identity (see Nassiri, fig. 4, secondary search stage 224; frame boundary and group ID; col. 8, lines 49-64) by determining a beginning of the SCH signal by identifying a chip location having a highest peak (see Nassiri, col. 8, lines 16-24, slot timing with highest peak).

Nassiri is silent to teaching that decoding the selected SCH signal by identifying a chip location having a highest signal to noise ration wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame. However, the claimed limitation is well known in the art as evidenced by Frigon and Yamaguchi.

In the same filed of endeavor, Frigon teaches that decoding the selected SCH signal by identifying a chip location having a highest signal to noise ratio (see Frigon, col. 7, lines 18-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nassiri with the teaching of Frigon in order to improve the synchronization process of cell search (see Frigon, col. 1, lines 30-35).

The combination of Nassiri and Frigon is silent to teaching that wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame. However, the claimed limitation is well known in the art as evidenced by Yamaguchi.

In the same field of endeavor, Yamaguchi teaches that wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame (see Yamaguchi, para. [0034] and [0037]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nassiri and Frigon with the teaching of Yamaguchi.

Regarding **claim 2**, the combination of Nassiri, Frigon and Yamaguchi also teaches the method of claim 1 wherein the SCH signal is transmitted in a predetermined timeslot of a system time frame and includes a primary synchronization code (PSC) transmitted in the timeslot at a predetermined chip offset (see Nassiri, fig. 3, primary stage 222) wherein the decoding includes determining a toffset at which the selected SCH is transmitted (see Nassiri, col. 8, lines 20-24, slot timing).

Regarding **claim 4**, the combination of Nassiri, Frigon and Yamaguchi also teaches the method of claim 2 wherein the chip with the highest signal to noise ratio is selected to obtain the location of the PSC sequence (see Frigon, col. 1, lines 30-35).

Regarding **claim 5**, the combination of Nassiri, Frigon and Yamaguchi also teaches the method of claim 4 wherein the location of the PSC sequence is adjusted to identify the chip location at which the PSC sequence begins (see Nassiri, primary stage 222, col. 8, lines 16-24, slot timing with highest peak).

Regarding **claim 7**, the combination of Nassiri, Frigon and Yamaguchi also teaches the method of claim 1 further including the step of identifying whether the chip location of the PSC sequence was derived from an even sample or an odd sample (see Nassiri, fig. 3, samples 310 and 320) where the PSC sequence is identified by processing a wireless communication signal at twice the chip rate (see Nassiri, col. 6, lines 53-54).

Regarding **claim 16**, Nassiri teaches a wireless transmit/receive unit (WTRU) configured to communicate with base stations of a wireless system the WTU receives an identifying synchronization channel (SCH) from at least one base station in a selected portion of a system time frame, the WTRU (see Nassiri, abstract and fig. 2) comprising:

a receiver configured to receive a wireless signal including at least one SCH signal (see Nassiri, col. 6, lines 1-5);

at least one correlator configured to identify received SCH signals using a power threshold (see Nassiri, fig. 3, primary search stage 222, col. 8, lines 4-15, peak detector

350) based on a plurality of chip samples sampled at twice the chip rate (see Nassiri, col. 6, lines 53-54);

a processor for selecting an identified SCH signal for decoding (see Nassiri, col. 8, lines 16-25, highest peak);

a processor for decoding the selected SCH signal to determine system time frame timing and base station identity (see Nassiri, fig. 4, secondary search stage 224; frame boundary and group ID; col. 8, lines 49-64) by determining a beginning of the SCH signal by identifying a chip location having a highest peak (see Nassiri, col. 8, lines 16-24, the slot timing with highest peak).

Nassiri is silent to teaching that the processor for decoding the selected SCH signal by identifying a chip location having a highest signal to noise ration wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame. However, the claimed limitation is well known in the art as evidenced by Frigon and Yamaguchi.

In the same filed of endeavor, Frigon teaches that the processor for decoding the selected SCH signal by identifying a chip location having a highest signal to noise ration (see Frigon, col. 7, lines 18-26).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nassiri with the teaching of Frigon in order to improve the synchronization process of cell search (see Frigon, col. 1, lines 30-35).

The combination of Nassiri and Frigon is silent to teaching that wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame. However, the claimed limitation is well known in the art as evidenced by Yamaguchi.

In the same field of endeavor, Yamaguchi teaches that wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame (see Yamaguchi, para. [0034] and [0037]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nassiri and Frigon with the teaching of Yamaguchi.

2. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nassiri, Frigon and Yamaguchi as applied to claim 2 above, and further in view of Willenegger.

Regarding **claim 3**, the combination of Nassiri, Frigon and Yamaguchi teaches the method of claim 2.

The combination of Nassiri, Frigon and Yamaguchi is silent to teaching that wherein the PSC having the highest power is detected by summing the peak PSC over four frames and dividing the summed power by an estimated noise value to obtain a signal to noise ratio for each chip in a frame. However, the claimed limitation is well known in the art as evidenced by Willenegger.

In the same field of endeavor, Willenegger teaches that wherein the PSC having the highest power is detected by summing the peak PSC over four frames (see Willenegger, fig. 6, col. 6, lines15-25) and dividing the summed power by an estimated noise value to obtain an signal to noise ratio for each chip in a frame (see Willenegger, fig. 9, component 408, col. 13, lines 40-44; col. 16, line 60-col. 17, line 10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teaching of Nassiri, Frigon and Yamaguchi with the teaching of Willenegger in order to reduce synch channel interference (see Willenegger, col. 1, lines 50-52).

Regarding **claim 6**, the combination of Nassiri, Frigon, Yamaguchi and Willenegger also teaches the method of claim 3 wherein the step of dividing is not implemented where the signal value is less than the threshold value (see Yamaguchi, para. [0037]).

Response to Arguments

Applicant's arguments filed 1/16/08 have been fully considered but they are not persuasive.

With respect to Claim 1, the Applicant argues that the combination of Nassiri, Frigon, and Yamaguchi does not teach or suggest the feature of "decoding the selected SCH signal to determine system time frame timing and base station identity by

determining a beginning of the SCH signal by identifying a chip location having a highest signal to noise ratio wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame". However, the Examiner respectfully disagrees.

More specifically, as cited in the Office Action, the combination Nassiri, Frigon, and Yamaguchi a method comprising:

decoding the selected SCH signal (see Nassiri, abstract, fig. 4, secondary search stage 224; col. 8, lines 49-64) to determine system time frame timing (a maximum peak of a frame boundary) and base station identity (group ID of the base station) by determining a beginning of the SCH signal by identifying a chip location (see Nassiri, col. 8, lines 16-24, slot timing with highest peak) having a highest signal to noise ratio (see Frigon, col. 7, lines 24-26; selecting highest SNR) wherein the noise is computed using a predetermined number of chips that is less than the total number of chips in a frame (see Yamaguchi, para. [0034] and [0037], first 256 chips in each 2560 chips).

Further, the Applicant argues that the combination of Nassiri, Frigon, and Yamaguchi does not teach or suggest receiving an identifying synchronization channel (SCH) signal from at least one base station at a predetermined chip rate in a selected portion of a system time frame. However, the Examiner disagrees.

More specifically, the Examiner submits that the combination of Nassiri, Frigon, and Yamaguchi teaches receiving an identifying synchronization channel (SCH) signal from at least one base station at a predetermined chip rate (see Nassiri, col. 6, lines 50-

55; chip rate at 3.84 MHz) in a selected portion of a system time frame (see Nassiri, col. 6, lines 61-63; beginning of each slot).

Lastly, the Applicant argues that the combination of Nassiri, Frigon, and Yamaguchi does not teach or suggest the feature of identifying received SCH signals using a power threshold. However, the Examiner respectfully disagrees.

More specifically, the Examiner submits that that the combination of Nassiri, Frigon, and Yamaguchi teaches the feature of identifying received SCH signals using a power threshold (see Nassiri, fig. 3, primary search stage 222, col. 8, lines 10-15, peak detector 350; a predetermined peak threshold value).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to WEN W. HUANG whose telephone number is (571)272-7852. The examiner can normally be reached on 10am - 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on (571) 272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/W. W. H./
Examiner, Art Unit 2618

/Matthew D. Anderson/
Supervisory Patent Examiner, Art Unit 2618